PATENT APPLICATION

HIGH OUTPUT POWER QUASI-SQUARE WAVE INVERTER CIRCUIT

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HIGH OUTPUT POWER QUASI-SQUARE WAVE INVERTER CIRCUIT

The invention described hereunder

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of power supplies and more particularly to the field of structures for holding and supporting power supply components that are required to withstand shock in the range of 100 Gs.

2. Description of Related Art

SUMMARY OF THE INVENTION

The invention shows that

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 - 27 are inclosed. Appendix pages 1-11 are photocopies of pages from Kamaran's notebook.

DETAILED DESCRIPTION

The invention is a HIGH OUTPUT POWER QUASI-SQUARE WAVE INVERTER CIRCUIT used in connection with a 28Vdc to 115 Vac 2.5 KW RUGGEDIZED INVERTER STUCTURE. The HIGH OUTPUT POWER QUASI-SQUARE WAVE INVERTER CIRCUIT and rugidized structure comprises a base, the base having a forward and rear rectangular tube separated by an integral base plate, the tubes and integral base plate being formed from rectangular aluminum having a thickness greater than 0.125 inches

A vertical U-Shaped frame formed from plate aluminum having a thickness of 0.187 inches spaced apart in parallel relation at a distance of approximately 18 inches. The U-Shaped frame having a left, right and rear wall, each wall having a respective inner and outer surface. The U-Shaped frame is integral in that the left and right walls are coupled

to opposing edges of the rear wall and it is homogenous in that it is formed from a single plate of aluminum having no joints, seams or welds.

The tubes and integral base plate operating to stiffen the base plate, the front and rear rectangular tubes extending across the rear of the base to couple the left side of the vertical U-Shaped frame to its right side.

A flat aluminum plate coupled to the top of the base. The flat aluminum plate is approximately 0.250 inches thick. The flat plate extends approximately 2/3 the distance between the left and right sides of the vertical U-Shaped frame which are separated by approximately 18 inches .

A toroidal transformer, having a diameter of about 9.5 inches is mounted to the flat aluminum plate. From mathworld.com. the word toroid characterizes a surface of revolution obtained by rotating a closed plane curve about an axis parallel to the plane which does not intersect the curve. The simplest toroid is the torus. The word is also used to refer to a toroidal polyhedron

The toroid core appears to be near fully wound except for a central hole region reserved for a mounting bolt. The toroid has a base surface, a top surface and the central hole. The space between the transformer base surface and the flat aluminum plate is filled with a thermally conductive resin. The resin is an epoxy filled with aluminum powder to enhance its thermal conductivity. The central hole of the toroid is filled with loaded epoxy except for the hole. The wire that is used is for the secondary is square in cross section and is believed to be number 10 wire. The temperature specified for the wire insulation is 200 degrees centigrade. That is class H for the transformer. Winding resistance, turns ratio, operating voltage and things like that are specified in a source control document that is used to purchase the transformer. The transformer is the main power transformer is secured to the plate by a hold down bolt that passes through a pre-cast hole in the loaded epoxy fill, the hole passing from the top surface of the toroid to the bottom surface.

A G-10 fiberglass-epoxy board plate, formed from fiberglass, the circuit board plate being positioned on the top surface of the toroid. Three left and right primary terminals on the plate are coupled to the left and right ends of the transformer's primary winding and an input center tap terminal is coupled to a primary winding center tap. Two output terminals are coupled to the left and right ends of the secondary winding. No center tap is used on the secondary. The secondary voltage is 120VAC nominally quasi-square wave or quasi-sine wave in shape and 60 Hz in frequency. The dead time is established by the third harmonic and is about three milliseconds. During the dead time, the OFF-TIME Shorting circuitry shorts the two ends of the primary winding together to form a temporary common node but does not short to common node to ground.

Heat is removed from the core and the copper wire in the window of the transformer via the thermally conductive potting material and then through the plate from which the heat is coupled to the base of the integral base plate in the base.

A left and right power module are coupled to respective left and right inner wall surfaces of the vertical U-shaped frame.

Each power module has a large aluminum base plate with a thickness of approximately 0.250 inches.

A power FET circuit board having an inner surface and an outer surface is coupled to each respective base plate. Each power FET circuit board has two rows of ten each IRF540; 100 V, 28A power MOSFETs coupled in two parallel sets. The first set is comprised of 16 of the 20 MOSFETs and the second set is comprised of the remaining 4 out of 20 MOSFETs. The set of 16 MOSFETs are used for the power switching, while the set of 4 MOSFETs are used for the Transformer OFF-TIME SHORTING.

Each FET has a metal mounting tab. Each FET has a plastic body coupled to the metal mounting tab Each FET has a Gate, a drain and a Source lead extending from its

respective plastic body. The drain lead of each FET is electrically common with its respective metal mounting tab.

The metal mounting tabs of each FET is pressed against a strip of insulating material that is coupled to the base plate. The insulating material is called ISOSTRATE, and is made by Power Devices Corporation, located in Laguna Hills, California. It is a type of pre-greased Kapton. The strip of insulating material prevents electrical contact between the drain and the large aluminum base plate. The three leads of each FET are formed for insertion into printed circuitry on the outer surface of the respective circuit board.

A strip of high durometer neoprene rubber material made by 3M Company, part number: SJ6008, is inserted between a plane formed by the plastic bodies of the FETs and the respective power FET circuit board outer surface. A high durometer rating implies that the material compresses only slightly under load.

Mounting screws being inserted through the power FET circuit board inner surface to its outer surface and then to the respective large aluminum base plate to force the power FET circuit board toward the respective large aluminum base plate, the neoprene strip being compressed between the power FET circuit board outer surface and the plastic bodies of the FETs, the plastic bodies transferring the load imposed by the neoprene strip to the metal tabs pre-loading the tabs against the insulation strip on the large aluminum base plate. Three screws are used to force the circuit board against the rubber strip and thence against the plastic bodies of the row of ten FETs thereby obtaining fairly even pressure.

A control module is coupled to the inner surface of one of the power FET circuit boards. Two bolts are used on the lower edge and three are used along the top edge. Two Z-shaped brackets are used.

Power cables pass through the rear wall of the vertical U-Shaped frame.

RUGGEDIZIDED 28Vdc to 115 Vac 2.5 KW INVERTER CIRCUIT was described by INVENTOR KAMRAN KAZEM in connection with the schematic he provided as follows.

The outputs are at 8C on the schematic to the power boards. The controller is an SG1526. Although it has an internal oscillator, we have used a crystal controlled oscillator for greater precision. I start with IC U4, a 4060 CMOS chip in conjunction with Crystal Y1 which is actually a tuning fork resonator. It is not an actual crystal. It oscillates at an audio frequency of 15.36 KHz.

The 15.36 KHz signal is divided down to 120 Hz at the sync input, pin 12 of U2, the SG1526 controller. U3B is a FF, an MC4013 that provides a divide by 2 function. On the input side of the U3B FF, the frequency is 240 Hz. At U4, the previous stage, the frequency is 480 Hz.

Current sensing is achieved using the on-resistance of the power FETs on the power boards. The signal is sensed and rectified by bridge BR1. The output of BR1 is passed to comparator U15C which compares the resulting rectified signal with a dc level that is adjusted using R63 to set the threshold level. The threshold is set to not exceed 2.5 volts.

The circuit is a synchronous circuit. The sense voltage is gated on when the FETs are conducting. U11 gets a signal from the main oscillator or U4 to gate the signal on as the FETs are driven into conduction. U15D is a one shot circuit. The MC1403 is a D-Flip Flop. The output of that U11B FF is the Overload Signal. The Q output of Q11B normally remains high. It goes low to indicate an overload. The flip flop is tied to the U4 master clock. Data gets clocked in every half cycle.

U15D is a timing circuit. It controls the time that the converter is allowed to continue to run for a few seconds after the detection of an over-current or fault condition. This delay accomodates the typical surge requirement of a motor starting into an initial locked rotor or the high input current to the filament of a lamp load.. A motor can come up to speed and run within a few seconds with not timer trip. If the over load continues past the time threshold, U15D timing circuit. It controls the D-input that is the data input to the U11B flip-flop. If the data is high, then it clocks through a high. That is its normal state. If a fault condition persists, it times out and goes low. That shuts the Inverter output down completely.

Moving to B6 on the schematic, and U15A and U15B. These Ics are used to sense input over voltage and under voltage. If the battery driving the 28V buss is too low, i.e. below 18 VDC, we terminate inverter operation so as not to kill the battery. If the battery voltage is above 33 VDC inverter operation is terminated to prevent output voltage over stress to the loads coupled to the outputs of the inverter.. A high input voltage with cause the inverter operation to shut down instantly. A low voltage detect signal will not terminate Inverter operation immediately to accommodate line drops due to high current start loads. The U15D timer controls the delay, which is set to about 7 seconds. Indicator lights are provided.

The reset circuit includes the U11B F/F that controls weather the unit is allowed to run or the output will be inhibited. A reset switch is shown between M17 at location A7 and signal M23 at location A5 that is also part of the timer. If after the Inverter is reset, you have a low battery, you discover that you have a low battery, capacitor C20 is part of the U15B timer, discharges terminating Inverter operation by driving the inverting input of U15D lower than the 6V reference.

In the case of a high input voltage situation, note that there is an additional diode D22 that goes right to capacitor C20 and will discharge it triggering the F/F U11 to go to the low state. That terminates operation instantly. The low battery detection circuitry does

not have a similar diode. The timing circuitry allows C20 to discharge through R47 and provides six to 7 seconds to allow the battery to come back up if the drop was due to a momentary surge.

The circuitry in the center of the drawing is the ac regulation circuitry. U16 is a quad LM324 Op Amp. Three stages are used in the AC Regulation Feedback Loop. In this push-pull design, as you might recall, the drains of the FETs or the collectors of bi-polar switches go to double the input voltage. We typically see twice the 28 Vdc level or 56 Volts peak there. The minimum voltage fed into the U16 circuit is the battery voltage of 28 VDC nominal. U16A is a level shifting circuit translating the 56 V peak level down to about 10V, and also translating the minimum level of 28V down to the control circuit reference level or circuit ground. Pin 1 of U16A is a divided down signal that goes from about 0 to 10 V that goes up and down with the output pulses. The result is an analog output voltage pulses that is referenced to control ground. That is fed to the inverting input of U16B, which adds a little DC into the signal that helps the load regulation.

U16C, the error-amp stage, is the main regulator that controls level of the AC output voltage to keep it at 120 VAC. On the non-inverting input of U16C pot R8 is the output voltage adjustment pot. The pot is supplied from a precision 12 V reference. The inverting input receives a signal from the output of U16A followed by U16B. The output of that, the 4016 analog switch is in series with the error amp output, U16C, so we can open that signal if we want to. That is then fed up to U2 the 1526 to control the pulse width. The control signal is a dc level in the range of 0 - 4 VDC

Off time shorting is partly generated by the sync signal from U2 because that signal is active both outputs of the 1526 are off. During that interval, both power board outputs are off. We take that signal to U17C to buffer it, then to U17A to invert it and it is then amplified by transistor Q3. The two PWM output signals are wired or'd together with diodes D26 and D42. The or'd signal is high when the outputs are high and low only when both outputs are low. That is the condition when we want the off-time shorting to be enabled.

Q3, is a 2N2907A small-signal transistor. The output of that goes through a series diode, D39 and feeds the gates of the off-time shorting transistors on both the left and right power boards, which shorts the two halves of the primary windings together, but not to ground to allow the primary current to re-circulate and degenerate to reset the core. This also helps keep the output waveform clean during the power transistor off-time.

A VIBRATION AND SHOCK TEST WAS MADE ABOUT MID AUGUST 7th and 8th 2001 which tests were witnessed by a government QAR representative from the Irvine, CA DCMO office.

None of the design existed in the proposal stage. You sent the proposal in before you came up with the schematic. Yes that is the case. There was development going on right up to the testing.

The use of the SG1526 helps reliability and reparability of the unit. The use of the military type crystal and the use of the high-current power FET driver IC, U9 at 5C on the drawing, allows us to cascade far more than the three inverters that the competition can put in parallel. We can cascade up to ten units, which contain about 400 power MOSFETs.

The toroid transformer uses a tape-wound silicon steel core.

Tape prepared on 07/21/02

Kamran Kazam,s comments on pages from his lab book, the pages starting from a date of 07/24/01. The page numbers in the log book did not come out in the copies. Page 67 starts the information entered on 07/24/01. The copies of the log book pages are numbered 1 - 10 at the bottom of each page.

In the middle of the page, the entry titled minimum changes required on the MDL (Magnetic Design Laboratories) control board. for TACOM test of 2.5 KW Inverter using 2.5 K bleeder. Referring to Fig. 1, add 2 each 1N4148 diodes. The diodes are circled on Fig. 1. The cathodes are common and are connected to M5, a test point. The diodes are designated D52 and D53. One anode goes to U14-11 and the other goes to U14-9. The second item on the page of the note book is add one each 1N4148 , cathode to U15-9 and the anode to U15-12. That diode is designated D47 on the schematic. It is not clear from the schematic subsection I am printing that will be titled page or Fig. 2. The U15-12 node provides a battery return signal or reference level with is the ground for the schematic. The purpose of D47 diode is to prevent negative spikes generated by the transformer from disrupting the current limiting function that is provided by U15-C located on Fig. 2 at A-7.5.

In the log book at the next subsection, we find "Replace D29 with a jumper. That change is also shown on Fig. 2 between the output of comparator U15 and the reset input to the load latch U11-B. The diode D29 diode is made necessary for the cascading of units that will occur in the Tank applications. D29 eliminates the isolation between the current comparator U15-C which is between the master and the slave. Very little of the control board circuitry in the slave has bias power to work. That is the one area where the slave

controls board circuit is powered up and functions. That is what we call the main current limit protection. That is what we call the main current limit comparator. So any slave unit that is being overloaded will shut down the other units including the master inverter. The control circuit in the master unit is used to control the pulse width modulation of all of the slave units. Interruption is controlled via the M2 signal right under the D29 diode as shown. So the D29 is replaced with a jumper.

Subsection 5 on the notes in the Log book: The next subsection in the notes at page 1, item 4 is an instruction to delete R48 as show on Fig. 3. The component is located between 17 C and D-24 located at A-5 on the schematic. It was not being used so the part was deleted.

The next log book entry delets R37 which is over in the idel circuit. The part or circuit is not used. The idel circuit is deleted to allow the cascaded military Tank units to operate properly since the outputs of each are separate.

Item 6 deletes R59 on Fig. 2 and appears beneath diode D-29 discussed above. It is a one meg resistor and its function again is related to the number of units to be cascaded.. If two units are cascaded, the value drops to 500K. At three units are connected, the value drops to 333K. The impedance gets too low and starts to discharge capacitor C-21 which is a critical timing cap for the current limit circuit. It discharges that cap too fast so rather than have that condition, we simply delete R59.

On log book page 68, page 2 in the copies, changes were listed as checked that were necessary for multiple unit operation. A note appears that informs that both have a 2.5 K ohm 10 W resistor on the control board on the bread board in an unused section. The function of the bleeder circuit is to insure that a sufficient minimum load is imposed to cause the idel circuit to think that the system is in the normal high output power state even when that is not the case. The idel circuit is set to trip at about 5 Watts.. If the load is under the trip level, the cirucit goes into a battery saving mode so that the battery is not discharged. The system drops the output voltage from 120 to 45 to 60 Vac. The

introduction of the bleeder resistors insures that the circuit will not enter the ide model.. However this plan did not work and other changes had to be made to obtain satisfactory operation.

On page 72 and 73 dated 7/25/01 have to do with testing a Harts brand Inverter.that came with a dual housing assembly from the Tank command. On page 74 in my lab book dated 07/25/01, at item one, at the top of page number 3. after the phrase "Fix startup out of ctl problem : Added 10K resistor from U48- 1 to U48-2 to help the control loop remain in control before of the reset signal. You would start up a first unit some times and it would start up not particularly in control.. The change was introduced to get the unit to start in a controlled and predictable manner. The addition of the 10K resistor from U8-1 to U8-2 was an attempt help the control loop stay in control before reset. This is an attempt to bi-pass the analog switch that is turned on and off by the idel circuit so that it will have at least a partial input from the error amplifier while it was in idel and as it comes out of idel during start up. You will see a circled area on Fig. 4 where the part was removed. There is a jumper there W10 that was inserted in place of the resistor at a later time.